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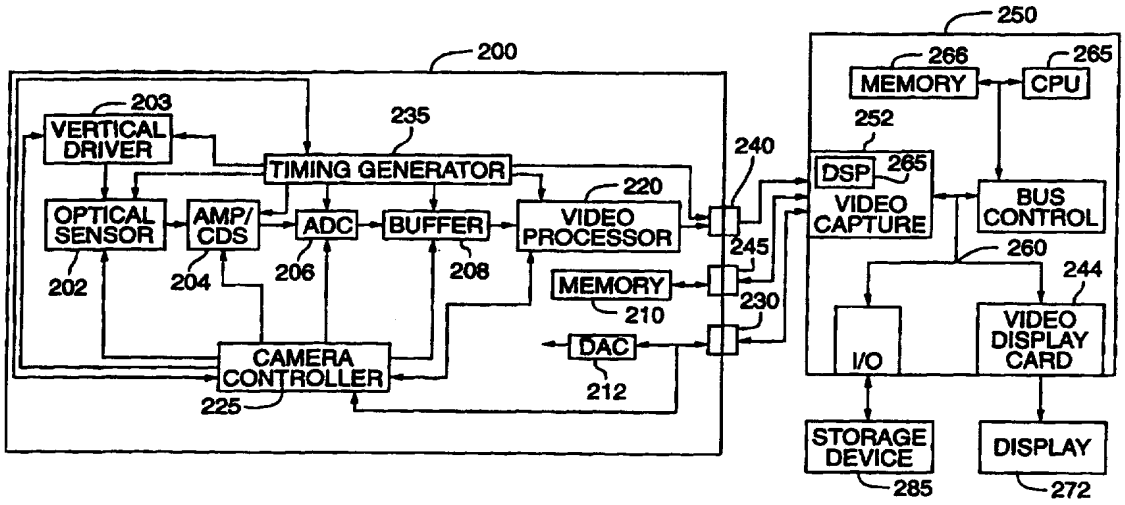

(57) Abstract

A digital video camera system for capturing digital video sequences for computer systems contains an optical sensor to capture images, an amplifying element to amplify the images, an analog-to-digital converter to convert the images to a digital format, a video processor to optimize the images for computer systems, and a digital video interface to output the digital video data. The digital video camera has independent frame rate, exposure time, scan rate, and resolution controls which can be dictated by the computer system so that the output of the digital video camera conforms to the requirements of the computer system rather than the requirements of analog video equipment.

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A DIGITAL VIDEO CAMERA SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates generally to digital video cameras and in particular to a digital video camera designed for use with microprocessor based devices, such as computers and video phones.

Description of the Related Art

As computers have improved in processing power, display capability, and storage capacity, computer applications incorporating digital video sequences have become commonplace. However, equipment to capture video sequences specifically for computer systems, including such microprocessor equipped devices as video phones, video surveillance systems, image recognition/inspection systems, and video diagnostic systems has not been developed.

Computer video sequences consist of a sequence of noninterlaced frames of digital pixel data. Typically the digital pixel data will be in YUV or RGB format. However, the typical video camera is designed to function with conventional video equipment and provides an analog video output, such as NTSC or PAL.

Figure 1 illustrates a conventional method of capturing a video sequence. Video camera 100, which

outputs an analog video signal, is connected to computer system 150. Video camera 100 contains charged coupled device (CCD) 102, to capture multiple images. The analog images of CCD 102 pass through amplifying element 104 and are converted into digital images by analog-to-digital converter 106. At this point the format of the digital images still corresponds to the physical space of the CCD (as explained below with respect to Figure 3). Digital signal processor (DSP) 108 converts the digital images from CCD physical space format into a display space format (as explained below with respect to Figure 3). The display space format images are then converted into an analog video signal by digital-to-analog converter 110. Microprocessor 112, controls the various components of video camera 100 using timing generator 114.

Video camera 100 is coupled to computer system 150. Specifically the analog output port of video camera 100 is connected to video capture card 152 in computer system 150. Video capture card 152 contains analog-to-digital converter 153, which converts the analog video signal into a digital video signal suitable for use by computer system 150. The digital video signal is then placed on computer bus 160 where it can be further processed by CPU 165, displayed on display 172 by video display card 174, or stored on storage device 185.

A major problem with the conventional system is that the analog video stream from video camera 100 provides more data than computer system 150 can process. For example an NTSC analog video stream provides data for 60 interlaced fields (30 frames) per second having resolution of approximately 720x492. However, computer system 150 typically requires data in non-interlaced frames and can only process the video data at a rate of about 15 frames per second with a resolution of approximately 320x240. Typically, computer system 150 will grab one frame and process it while some number of subsequent frames,which can not be processed, are dropped. Therefore, computer 150 only captures a subset of the actual analog video sequence which will result in a very "jerky" digital video sequence. Furthermore, the quality of the resulting video sequence is degraded by the multiple conversions from analog to digital to analog and then back to digital format.

Hence there is a need for a method or apparatus to produce a video signal for a computer system based on the needs of the computer system rather than the needs of analog video equipment.

SUMMARY OF THE INVENTION

In accordance with this invention, a digital video camera is provided to meet the demands of a computer

system instead of analog video equipment. Instead of outputing video data in standard analog video format, the digital video camera provides a digital video signal at the frame rate and resolution dictated by the computer system.

Specifically, in one embodiment a digital video camera has an optical sensor to capture images, an amplifying element to amplify the captured images to a proper brightness level, an analog-to-digital converter to digitize the images, a video processor to transform the images for use with the computer system, and a digital output port to send the digital video images to the computer system. The computer system is able to dictate the frame rate, scan rate, resolution, exposure time and analog signal gain of the digital video camera. By independently controlling exposure time, scan rate, and analog signal gain, the computer system of this invention can use the optical sensor of the digital video camera as an analog frame buffer to obtain temporal smoothing within each frame of the video sequence. The resulting video is smoother than can be obtained from conventional video cameras.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a conventional video camera attached to a computer system.

Figure 2(a) shows a digital video camera in

accordance with one embodiment of the present invention attached to a computer system.

Figure 2(b) shows a video phone system using digital video cameras according to one embodiment of the present invention.

Figure 3 shows CCD area sensors which can be used as the optical sensor in a digital video camera in accordance with one embodiment of the present invention and the corresponding display space of the CCD area sensor.

Figure 4 shows various image manipulations which can be performed in a digital video camera in accordance with one embodiment of the present invention.

Figures 5, 6, and 7 show the schematics of a digital video camera in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

According to the principles of this invention, certain limitations imposed by conventional video cameras have been overcome. The present invention provides digital video data at the resolution and frame rate dictated by the computer system. For example, in one embodiment of the invention, after receiving signals from the computer system, which specify the frame rate and resolution of the digital video images,

the invention will control an optical sensor such as a CCD to capture images at the specified frame rate and resolution, convert the images to digital format, and send the images to the computer system. Furthermore, the computer system can control the scan rate and exposure time of the optical sensor as well as the analog signal gain on the output of the optical sensor to achieve temporal smoothing.

Figure 2(a) shows video camera 200 connected to computer system 250 according to one embodiment of the present invention. Video camera 200 has optical sensor 202, which captures a sequence of analog images and outputs the images to amplifying element 204. In some embodiments, optical sensor 202 is controlled by vertical driver 203 which receives timing controls from timing generator 225. Amplifying element 204, of well known design amplifies each of the images with a controllable analog signal gain to form amplified images. If optical sensor 202 uses CCD's, amplifying element 204 can also perform correlated double sampling to eliminate drift in the charge amplifier of the CCD. Specifically, the CCD outputs the video data in two parts where the difference between the parts is the actual video data. Any drift in the charge amplifier would effect both parts equally and is eliminated by subtracting the two parts. Therefore, amplifying element 204 subtracts the voltage output of the first

half of the data sample from the voltage output of the second half of the data sample of the CCD, if correlated double sampling is required.

Analog-to-digital converter 206 converts the analog images into digital images in sensor physical space format. Typically, the sensor physical space format has a resolution of eight bits per pixel. In some embodiments of the camera, buffer 208 is included so that video processor 220 can sample data from buffer 208 at a different rate than the scanning rate of optical sensor 202.

Video processor 220 process the digital images under the direction of camera controller 225, and sends the processed digital images in sensor physical space format to computer system 250. In some embodiments of video camera 200, video processor 220 also converts the processed digital images into display space format.

Specifically, in one embodiment, the eight bit pixels are processed to correct for any non-linearities or conversion errors in optical sensor 202, amplifying element 204, or analog-to-digital converter 206, using well known techniques. The eight bit pixels are then multiplexed into two sequential nibbles in big-endian fashion. The horizontal and vertical sync signals are also encoded into the video stream. Furthermore, a timing signal is sent with the video stream so that computer system 250 does not require a clock recovery

circuit.

Camera controller 225 receives control signals from computer system 250 through control interface 230. Digital-to-analog converter 212 converts digital controls to analog control signals, so that computer system 250 can also control the analog portions of video camera 200. Camera controller 225 in conjunction with timing generator 235 controls optical sensor 202, vertical driver 203, amplifying element 204, analog to digital controller 206, buffer 208, and video processor 220. In some embodiments of video camera 200, non volatile memory device 210, which could be for example an EEPROM or a flash memory device, is included to provide computer system 250 with "factory default" settings such as optical sensor biases, gains, and timing, as well as the color calibration for the particular optical sensor in video camera 200. In addition, for some embodiments of video camera 200, various components will be combined into a single integrated circuit. For example, video processor 220, camera controller 225, and timing generator 235 could be combined onto a single ASIC.

The processed digital images of camera 200 pass through digital output interface 240, which is connected to video capture card 252 in computer system 250. Video capture card 252 converts the processed digital images into a display space format

such as YUV or RGB for use by computer 250, if necessary. The display space format digital images are then transferred on computer bus 260 to be further processed by CPU 265, displayed on display 272 by video display card 244, or stored on storage device 285. Alternatively, video capture card 252 can pass the sensor physical space format images onto computer bus 260 and allow CPU 265 to convert the images into display space format using software stored in memory 266.

Computer system 250 can be replaced by other devices, such as video phones or set top boxes, which require video images. Figure 2(b) shows two video phones using cameras according to the present invention. With video phone applications, the limiting factor on the quality of the video (i.e. frame rate and resolution) is the quality of the telephone connection over standard analog telephone lines. As shown in Figure 2(b), video phone 295 is connected to video phone 296 over telephone network 290. Newer phone technology such as ISDN can be used as well. Furthermore, video conferencing can also be performed over a local area network instead of using a standard telephone line. After a connection between the phones is established, the quality of the connection is determined by sending standardized test patterns between the phones at decreasing rates until a

satisfactory connection is established. After the quality of the connection is determined, video phone 295 instructs video camera 291 to feed video images at a frame rate and resolution that can be supported over telephone network 290. Similarly, video phone 296 will instruct video camera 298 to feed video images at a specific frame rate and resolution. Typically both cameras will use the same frame rate and resolution, but in some cases where the video from one side of the phone connection is more important than the other side, different frame rates and resolutions can be used. Since the quality of the connection over telephone network 290 will vary from call to call, it is imperative that video phones be able to control the frame rate and resolution of the incoming video stream.

Video phone 295 combines the video signal from video camera 291 with an audio signal from microphone 292 and transmits the resulting combined signal to video phone 296 over telephone network 290. Video phone 296 will decode the signal from video phone 295 and display the video data on display 297 and play the audio data on speaker 299. Similarly, the video data from video camera 298 will appear on display 293 associated with video phone 295, while the audio data from microphone 289 will be played on speaker 294.

In video camera 200 (Figure 2(a)), optical

sensor 202 can be for example a CCD area sensor array, an array of active or passive photodiodes, or an array of charge injection devices. However, the most commonly used optical sensor for imaging applications is the CCD area sensor array. Figure 3 shows schematically CCD area sensor array 300 which can be used as optical sensor 202. CCD area sensor array 300 contains a two dimensional array of photosites each of which provides an analog signal based on the amount of light on the photosite. Color filters are placed on the photosites so that each two by two grid of photosites can sense both the brightness and color of the impinging image. For CCD area sensor array 300 the four colors are cyan (Cy), magenta (Mg), Yellow (Ye), and green (Gn). However, other color schemes may be used such as RGB stripe as shown in CCD area sensor array 300a or RGB Bayer as shown in CCD area sensor array 300b. Each two by two grid of photosites of CCD area sensor array 300 correspond to one pixel in display image 320 which is made up of display pixels.

The arrangement of the photosites and color filters define the sensor physical space format which consists of a two dimensional array of the value of each photosite. Each two by two grid in the sensor physical space corresponds to one pixel in the display space. For example, box 330 containing cyan photosite 331, yellow photosite 332, magenta

photosite 333, and green photosite 334 corresponds to display pixel 350. Each photosite of CCD area sensor array 300 is used for multiple display pixels. Therefore, cyan photosite 331 and magenta photosite 333 in addition to yellow photosite 342 and green photosite 343 correspond to display pixel 360.

Unlike conventional video cameras, video camera 200 (Figure 2(a)) is not constrained to output a video stream based on an analog video standard. Therefore, camera controller 225 can control optical sensor 202 based on the requirements of computer system 250 rather than the requirements of standard video equipment. For example, since computer system 250 may not be able to handle 30 frames per seconds, camera controller 225 can set the scan rate of the optical sensor to achieve the desired frame rate. Furthermore, camera controller 225 can set the exposure time of optical sensor 202 independently of the scan rate.

Several benefits are derived from the ability to control scan rate and exposure time independently on optical sensor 202. By lowering the scan rate, optical sensor 202 is able to collect light for a longer time on each image and create a brighter analog image for amplifying element 204. Camera controller 225 can then lower the analog gain of amplifying element 204 resulting in less noise in the amplified image without

loss of brightness.

Another benefit of the reduced scan rate is that optical sensor 202 provides temporal averaging in each frame of the video. As explained above, conventional video capture systems drop frames when the speed of the video signal is too high, resulting in a "jerky" video. For example, a conventional system may capture only every other frame of a 30 frame per second video sequence to get a video sequence at 15 frames per second. Each frame is sampled in 1/30th of a second; thus the resulting 15 frames only contain half of the information captured by the optical sensor. In video camera 200, optical sensor 202 can sample each frame for 1/15th of second. The resulting 15 frames contain all of the information captured by optical sensor 202 thereby providing a "smoother" video sequence. By controlling the exposure time of optical sensor 202 and analog gain control of amplifier 204 independently of the scan rate of optical sensor 202, the amount of temporal averaging in the frames can be adjusted without loss of brightness in the video signal.

Another benefit of not being constrained to output a standard analog video signal is that video camera 200 can provide a digital video stream at the resolution required by computer system 250. As explained above, a standard analog video signal has a higher resolution than can be processed by computer system 250.

Therefore, it is desirable to reduce the resolution of the frames in the video before they are sent to the computer system. The simplest way to reduce the resolution is to subsample the pixels of the image. Figure 4(a) illustrates spread subsampling of the image. Each square 405-i (where i is an integer) in Figure 4(a) represents a pixel in display space format. Only the shaded squares 405-1, 405-3, 405-5, 405-7, 405-17, 405-19, 405-21, 405-23, 405-33, 405-35, 405-37, and 405-39 are actually sent to computer system 250. Thus, if optical sensor 202 captures images at a resolution of 640x480, subsampling as illustrated in Figure 4(a) would reduce the image to 320x240. Figure 4(a) illustrates subsampling in display space format for ease of understanding. However, the actual subsampling can be performed in sensor physical space format by optical sensor 202 or video processor 220 in order to reduce the amount of data that must be sent to computer system 250. Other patterns of subsampling are also possible. The specific subsampling pattern is dictated by computer system 250 to camera controller 225. This is accomplished by adjusting the row and column addressing and timing of optical sensor 202. Also if necessary, buffering by buffer 208 for output formatting is also performed.

Another useful reduction method is to only send a part of the full image, also known as contiguous

subsampling. As shown in Figure 4(b), rectangular window 410 containing only a part of captured image 420 as captured by optical sensor 202 is sent to computer system 250. Placement and size of rectangular window 410 is controlled by camera controller 225 under direction of computer system 250. This allows computer system 250 to simulate zooming, paning (i.e. moving the camera horizontally), and tilting (moving the camera vertically) without requiring physical manipulation of video camera 200. Reduction to rectangular window 410 can be performed in optical sensor 202 or video processor 220.

If the entire field of vision of video camera 200 is desired and spread subsampling does not yield an acceptable image, scaling of the captured image is performed by optical sensor 202 or video processor 220. Figure 4(c) illustrates the scaling or decimation of an 8x6 image into a 4x3 image. Each row of reduced image 430 is a weighted average of the rows of original image 440. Similarly, each column of reduced image 430 is a weighted average of the columns of original image 440. Thus each pixel in reduced image 430 is a weighted average of the pixels in an area of original image 440 corresponding to the pixel of the reduced image.

For example, row i of reduced image 430 is formed with the weighing factors (0.5, 0.5, 0, 0 ,0 , 0) so

that row i of reduced image 430 is formed by summing the rows of original image 440 multiplied by the corresponding weighing factor. Therefore row i of reduced image 430 is calculated by the following equation where r1-r6 are row 1-row 6 of original image 440:

$$(0.5*r1)+(0.5*r2)+(0*r3)+(0*r4)+(0*r5)+(0*r6)$$

Similarly, row ii of reduced image 430 is formed with weighing factors (0, 0, 0.5, 0.5, 0, 0); and row iii of reduced image 430 with weighing factors (0, 0, 0, 0, 0.5, 0.5). Column α of reduced image 430 is formed with the weighing factors (0.5, 0.5, 0, 0, 0, 0, 0, 0) so that column α of reduced image 430 is an average of column A and column B of original image 430. Column β of reduced image 430 would be an average of column C and column D of original image 440. Column γ of reduced image 430 would be an average of column 5 and column 6 of original image 440; and column δ of reduced image 430 would be an average of column 7 and column 8 of original image 440. The rows and columns can be averaged simultaneously or sequentially without changing the result. In this example, pixel (α,1) of reduced image 430 is formed by the average of pixels (A,1), (A,2), (B,1), and (B,2) of original image 440.

The specific weighing factors used are selected

by computer system 250, using such criteria as frame size requirements, brightness, processing time, and bandwidth of the connection to computer system 250. For example, if the brightness of the image needs to be increased, the weighing factors are increased so that the sum of the weighing factors for each row or column is greater than one. Similarly, an image can be darkened by lowering the weighing factors so that the sum of the weighing factors for each row or column is less than one. It is also possible to scale an image to a larger size by defining more weighted average rows or columns than original rows and columns.

Video camera 200 (Figure 2(a)) has various control and data interfaces for connection with computer system 250. Digital output interface 240 outputs the digital video image stream. Control interface 230 carries signals from computer system 250 which dictates the frame rate, frame size, analog gain, exposure time, frame format, and other control parameters of video camera 200. Auxiliary interface 245 is used to pass information and control signals between video camera 200 and computer system 250. The various interfaces of video camera 200 can be serial or parallel. Proprietary interfaces can be used on the various interfaces, as well as interfaces conforming to standards such as I2C or universal serial bus. Furthermore, the various interfaces of video camera 200

can also be combined to use a single proprietary or standardized interface.

Computer system 250 (Figure 2(a)), receives the digital video images on video capture card 252. Since video camera 200 outputs the digital video images in sensor physical space format, the digital video images must be converted into display space format. In some embodiments, video capture card 260 contains digital signal processor (DSP) 266 to perform the conversion. Alternatively, computer system 250 can perform the conversion in software running on CPU 265. Furthermore, with embodiments of video camera 200 using a standard interface, such as universal serial bus, a separate video capture card is not required.

A detailed schematic of a camera according to one embodiment of the invention is presented in Figures 5-7. Each schematic of Figures 5-7 is a separate printed circuit board. The three boards are connected through connectors as shown in the schematics. The circuit boards have separate power for analog elements and digital elements; however, the analog elements and digital elements share a common ground. Analog voltage levels are written as xxVA instead of just xxV, e.g. +15VA, instead of +15V. Furthermore as used herein signal names followed by "/" denotes an active low signal. For example "OE/" is an active low output enable signal.

Figure 5 shows the schematics of the optical capture board. Connector P101 connects the optical capture board to the control board of Figure 6. The signals on connector P101 are described with respect to the source or destination of the signals rather than at the connector. Capacitor C121 performs power decoupling between power signal +15VA and ground.

VDRIVE chip U121, which is a Panasonic MN3110SA, corresponds to vertical driver 203 (Figure 2(a)). VDRIVE chip U121 converts input signals PV1, PV2, PV3, PV4, (from EYECAM chip U215 of Figure 6) on input pins Viϕ1, Viϕ2, Viϕ3, and Viϕ4, to output signals OV1, OV2, OV3, and OV4, on output pins Voϕ1, Voϕ2, Voϕ3, and Voϕ4, respectively. Input signals PV1, PV2, PV3, and PV4 with input signals PVX1 and PVX3 represents the four phases of the vertical shift clock using only 0 volts and +5 volts. Output signals OV1, OV2, OV3, and OV4 are the four phases of the vertical shift clock to CCD U101 with the proper voltage levels required by CCD U101. The specific relationship for the phases of the vertical shift clock can be found in the data sheet for the CCD used, which in this embodiment is a Sharp LZ23313H5. Signals OV1, and OV3 have three possible output values, -9 volts, 0 volts, or +15 volts; therefore, input signals PVX1 and PVX3 (from Eyecam chip U215) are also provided on input pins CH1 and CH2, respectively. Specifically, if input signal PVX1 is

high (logic 5 volts) output signal OV1 will be set to +15 volts. IF input signal PVX1 is low, output signal OV1 is controlled by input signal PV1. Output signal OV3 behaves similarly with respect to input signals PVX3 and PV3. Except as noted above, if input signal PV1 is 0 volts, output signal OV1 is -9 volts. If input signal PV1 is +5 volts, output signal OV1 is 0 volts. Output signals OV2, OV3, and OV4 bears similar relationships to input signals PV2, PV3, and PV4 respectively. Output signal OSUB on output pin Osub is a 24 volt peak-to-peak signal which is used to completely discharge all the photosite on CCD U101. Output signal OSUB can be used to control the exposure time of CCD U101. The value of output signal OSUB is controlled by input signal PSUB (from Eyecam chip U215) on input pin ISub. If input signal PSUB is 0 volts, output signal OSUB is -9 volts. If input signal PSUB is +5 volts, output signal OSUB is +15 volts.

Input pin VH, which determines the high level power of output pins Voϕ1 and Voϕ3, is connected to power signal +15VA. Input pin VHH, which determines the high level power output of output pin Osub, is connected to power signal +15VA. Input pin VL, which determines the low level power of all the output pins, is connected to power signal -9VA. Input pin VCC, the logic high input level, is connected to power signal +5V. Input pin VM24, which determines the mid

level power of output pins Voϕ2 and Voϕ4, is connected to ground. Input pin VM13, which determines the mid level power of output pins Voϕ1 and Voϕ3, is connected to ground.

Resistor R121 provides decoupling between power signal +5V and switching noise generated by VDRIVE chip U121. Capacitor C122 is a decoupling capacitor between power signal +5V and ground.

CCD U101, corresponding to optical sensor 202 (Figure 2(a)) is a Sharp LZ2313H5. Detailed description of this CCD is available from Sharp. Input signals H1-F and H2-F on input pins Hiϕ1 and Hiϕ2, respectively, are filtered versions of the two phases of the horizontal shift clock from Eyecam chip U215 (Figure 6). Input pins Vϕ1, Vϕ2, Vϕ3, and Vϕ4, receives input signals OV1, OV2, OV3, and OV4, from VDRIVE chip U121, which are the four phases of the vertical shift clock. The scan rate of CCD U101 is determined by the frequency of the horizontal shift clocks and the vertical shift clocks. To reduce the scan rate of CCD U101, the frequency of the horizontal shift clocks are reduced. Furthermore, the frequency of the vertical shift clocks and reset gate signal RG must be reduced proportionately. In addition the frequency on other signals in the camera such as signals ADclk, ADclmp, CDS-CLMP, and CDS-S/H, should also be reduced. All of these signals are under

control of EYECAM chip U215; therefore, EYECAM chip U215 can control the scan rate of CCD U101.

Input pin RS clears the charge amplifier of CCD U101 in between the generation of pixels. Reset gate signal RG from EYECAM chip U215 (Figure 6) is coupled through AC coupling capacitor C123 (Figure 5) to input pin RS of CCD U101. Resistors R122 and R123 form a voltage divider which divides output signal RG-C from DAC chip U302 (Figure 7) to bias the level of the reset gate in CCD U101. The reset gate bias varies between individual CCDs. Each CCD must be measured for the optimum reset gate bias. The biasing information for the specific CCD is encoded into EEPROM U301 (Figure 7).

Input pin OFD, the overflow drain also known as the substrate bias, is used in the antiblooming structure of CCD U101. The substrate bias varies between individual CCDs. Each CCD must be measured for the optimum substrate bias. The biasing information for the specific CCD is encoded into EEPROM U301 (Figure 7). Input signal SUB is generated by circuits in Figure 7 which is described below. Input pin OFD is also used to completely discharge the photosites. This is accomplished as described above with input signal OSUB which is connected through AC coupling capacitor C124. Capacitor C101 provides filtering to the signal on input pin OFD.

Input pin PW is a power input for a P-Well structure within CCD U101 which requires a -9 volt power signal. Power signal -9VA is generated by a circuit depicted on Figure 7, which is described below. Zener diode d101 regulates power signal -9VA. Capacitors C105 and C106 provides filtering and decoupling between the power signal -9VA and ground.

Input pin T1 is a test pin which is tied to power signal +15VA during normal operations. Input pins OD and RD are the output transistor drain and the reset transistor drains, respectively. During normal operations input pins OD and RD are connected to power signal +15VA. Capacitor C104 provides decoupling between power signal +15VA and ground. The two pins labeled NC are no connects on the Sharp LZ2313H5. However, a compatible Panasonic model of the CCD requires decoupling capacitors C102 and C103.

Output pin OS of CCD U101, which is the video output pin of CCD U101, produces output signal VOUT. Signal VOUT drives the base of buffering transistor Q100; in this circuit transistor Q100 is a 2N3904. The collector of transistor Q100 is coupled to power signal +15VA. The signal from the emitter of transistor Q100 is coupled to CDS Chip U110 through AC coupling capacitor C110. Resistor R103 is an emitter load resistor.

CDS chip U110, which corresponds to amplifying

element 204 (Figure 2(a)), performs correlated double sampling as well as amplification. CDS chip U110 is a Sharp IR3P66. Detailed information about this chip is available from Sharp. Input pin IN receives an input video signal from CCD U101 through transistor Q100 and capacitor C110.

Input pin CBIAS of CDS chip U110, which provides the reference voltage to clamp the feedthrough level of the input signal, is coupled to ground through capacitor C111. Input pin ABIAS of CDS chip U110, which provides the bias level for the amplifier in CDS chip U110, is coupled to ground through capacitor C112.

Input pin S/H of CDS chip U110 receives sample and hold signal CDS-S/H from EYECAM chip U215 (Figure 6). Sample and hold signal CDS-S/H controls the sampling and hold circuits of CDS chip 110. Input pin CLMP of CDS U110 receives clamping signal CDS-CLMP from EYECAM chip U215. Clamping signal CDS-CLMP controls the clamping of the input signal to CDS chip U110.

Input pin GADJ of CDS U110 provides an automatic gain control. Signal CDS-GAIN is generated by DAC chip U302 in Figure 7 under control of computer system 250 (Figure 2(a)). Resister R111 and Capacitor C115 performs noise filtering on the CDS-GAIN signal.

The various power pins Vcc1-4 of CDS U110 are connected to power signal +5VA. The ground pins Gnd1-GND4 of CDS U110 are connected to ground.

Decoupling capacitor C114 is coupled between power signal +5VA and ground.

Output pin OUT of CDS U110 provides the output video signal CDS-VID. Resistor R110 is a load resistor on the output video signal.

Figure 6 shows the schematic of the control board of this camera. ADC chip U205, which corresponds to analog-to-digital converter 206 (Figure 2(a)), is a three input, eight bit analog-to-digital converter from Philips Semiconductor, part number TDA8709A. Only one of the inputs of ADC U205 is used in the circuit of Figure 6. Input pin Vin0 of ADC chip U205 is coupled to output pin OUT of CDS chip U110 through AC coupling capacitor C200. Input pins Vin1 and Vin2 are unused. Select input pins S0 and S1 are connected to ground to permanently select input pin Vin0 as the input source.

Output pin AnOUT and input pin ADCIN of ADC chip U205 provides a method for performing low pass filtering. The low pass filtering option is not used in the camera of Figures 5-7. However biasing resisters R200 and R201 are still required. Input pin A+5 is an analog power pin attached to power signal +5VA. Capacitors C201 and C202 provides decoupling between power signal +5VA and ground. Input pin ClmpCap controls black level clamping and is connected to ground through capacitor C203. Input pin CLP receives signal ADCLMP from EYECAM chip U215 (Figure

6), which provides a clamping pulse to ADC chip U205. Input pin Gain receives signal A/D-GAIN from the DAC chip U302 (Figure 7) to provide a gain control on ADC chip U205. ADC chip U205 has a separate analog ground Agnd and digital ground Dgnd; however as explained above, the circuit board uses a combined analog and digital ground. Consequently both analog ground Agnd and digital ground Dgnd of ADC chip U205 is connected to the single ground of the circuit board. Input pin Dec is a decoupling input which is connected to ground through decoupling capacitor C205.

Input pin CLK of ADC chip U205 receives signal ADClk from EYECAM chip U215 (Figure 6). Signal ADClk controls the timing and conversion rate of ADC chip U205. Resistor R203 and capacitor C207 filters signal ADClk; furthermore, resistor R203 provides some decoupling. Power input pins VCCD and VCCO of ADC chip U205 receive power signal +5VA. Resistor R202 and capacitor C206 provides filtering and decoupling.

Input pin CLS of ADC chip U205, the clamp level selection pin, is connected to ground. Input pin Format of ADC chip U205, the output format selection pin, is connected to ground. Input pin OE/ is the active low output enable pin. Since the outputs can be enabled continuously in this camera, input pin OE/ is connected to ground. Output pins D0-D7 of ADC chip U205 provide the 8 bit digital output of ADC chip U205.

Voltage regulator U201, in this implementation Linear Technologies LT1121CST-5, generates the analog 5 volt power signal +5VA from power signal +8VUR, which is generated from the circuits depicted in Figure 7. Capacitor C210 provides decoupling between power signal +8VUR and ground.

Interface J202, provides the interface between the camera of Figures 5-7 and computer system 250 (Figure 2(a)). Interface J202 corresponds to digital output interface 240, auxiliary interface 245, control interface 230. Signals SDA-F and SCL-F are the data and clock lines of the I2C bi-directional serial Bus, designed by Philips Corporation. The -F designation refers to the signals before they are filtered. Signals MD-0 to MD-4 are the outgoing digital video data signals. The 8 bit color data of each photosite are split into two four bit nibbles to be sent out. Signal MD-CK is the clock which accompanies the digital data. Power and ground from computer system 250 are received by the camera through interface J202.

The I2C serial bus uses open drain drivers therefore a pull-up resistor is coupled to the signals. Specifically pull up resistor R210 is coupled between power signal +5V and signal SDA-F and pull-up resistor R212 is coupled between power signal +5V and signal SCL-F. Resistor R211 and capacitor C211 filter signal SDA-F to provide signal SDA. Similarly,

resistor R213 and capacitor C212 filter signal SCL-F to provide signal SCL.

Oscillator U210 provides clock signal GCLK to EYECAM chip U215. Decoupling capacitor C213 is coupled between power signal +5V and ground. The frequency of Oscillator U210 is dependent on the video standard and resolution of CCD U101. For an NTSC CCD with a horizontal resolution of 512 pixels the frequency should be 39.2727MHz. For an NTSC CCD with a horizontal resolution of 768 pixels the frequency should be 57.2727 Mhz. For PAL CCDs the frequency should be 39 Mhz and 56.875 Mhz for horizontal resolutions of 512 and 768 pixels, respectively.

EYECAM chip U215 is a GEC Plessey series 80,000 ASIC. EYECAM chip U215 incorporates the functionality of video processor 220, camera controller 225, and timing generator 235 (Figure 2(a)). Furthermore, EYECAM chip U215 includes an I2C serial interface. The I2C serial interface in EYECAM chip U215 allows computer system 250 (Figure 2(a)) to control EYECAM chip U215. Computer system 250 can dictate the frame rate and resolution of the video to EYECAM chip U215. Furthermore, computer system 250 can use EYECAM chip U215 to control the scan rate and exposure time of CCD U101. The majority of the signals coupled to EYECAM chip U215 are explained in detail above. Therefore, only a brief description of the signals are presented

in this section.

Input pin CLKI of EYECAM chip U215 receives a clock signal from oscillator U210. As explained above, the frequency of the clock signal depends upon the video mode and resolution of CCD U101. Input pins ADI0-ADI7 receive the digitized video data from ADC chip U205. Output pins ADCK and ADCL provide control signals to ADC chip U205, as explained above.

Input pins CTI0, CTI1, and CTI2 of EYECAM chip U215 are general purpose input pins that are not used in the camera of Figures 5-7. Therefore, these input pins are connected to ground. Series resistors R220, R221 and R222 are used to prevent switching noise generated by EYECAM chip U215 from affecting the ground signal.

Input pins IAD1, IAD2, and IAD3 of EYECAM chip U215 are address offsets for the I2C interface built into EYECAM chip U215. The base address of EYECAM chip U215 is 60h, input pins IAD1, IAD2, and IAD3 allows selection of address ranging from 60h to 6Eh in increments of 2. In this embodiment IAD1, IAD2, and IAD3 are coupled to ground through series resistors R223, R224, and R225, respectively. Therefore, for this embodiment EYECAM chip U215 has I2C address 60h.

Output pins CPD0-CPD3 provide digital output signals MD-0 through MD-3. As explained above, signals MD-0 through MD-3 are nibbles of data from the digital

output stream. Series resistors R226, R227, R228, and R229 reduce noise on the data bus. Output pin CPCK provides clock signal MD-CK through noise reducing series resistor R230. As explained above, clock signal MD-CK provides timing for data signals MD-0 through MD-3.

Input pins SCLI, SDAI, SDAO, and SDMN of EYECAM chip U215 are used for the I2C interface built into EYECAM chip U215. Input pin SCLI receives the filtered I2C clock signal SCL. Input pin SDAI receives the filtered I2C data signal SDA. Output pin SDAO, an open drain driver, provides an unfiltered outgoing I2C data signal on signal SDA-F. Output pin SDMN provides an I2C serial data monitor signal, which can be used to determine the state of output pin SDAO.

Input pin RST/ of EYECAM chip U215 is an active low reset pin. Input pin RST/ is connected to a common power on/reset circuit comprising resistor R231, capacitor C214 and diode connected transistor Q201. Transistor Q201 has part number 2N3904. When power is first applied to the circuit the reset signal RST/ rises slowly with an RC time constant of approximately 22 msec. When power is removed diode connected transistor Q201 discharges capacitor C214 quickly.

Input pins TVO, TVF, TMI, and TSC of EYECAM chip U215 are test pins which are only used during manufacturing of EYECAM chip U215. During normal

operations input pins TVO, TVF, TMI, and TSC are connected to ground.

Ground pins GND are connected to ground. Power pins VCC are connected to power signal +5V. Decoupling capacitors C220-C227 are connected between power signal +5V and ground near power pins VCC. Decoupling capacitor C228 also provides decoupling between power signal +5V and ground for EYECAM chip U215.

Output pins H1 and H2 of EYECAM chip U215 provide the two phases of the horizontal shift clock to CCD U101. Resistor R232 filters noise out of signal H1 to provide filtered output H1-F. Similarly, resistor R233 filters noise out of signal H2 to provide filtered output H2-F. Output pins PV1-PV4, PVX1 and PVX2 provides the four phases of the vertical shift clock to CCD 101 through VDRIVE U121, as explained above.

As explained above, output pin PSUB provides signal PSUB to VDRIVE U121, which converts signal PSUB to signal OSUB. Signal OSUB is used to control the exposure time on CCD U101 (Figure 5). Therefore EYECAM chip U215 can control the exposure time on CCD U101 with signal PSUB. Since EYECAM chip U215 has control of the scan rate and exposure time of CCD U101, EYECAM chip U215 can use CCD U101 as an analog frame buffer to achieve temporal smoothing of the video signal.

Output pin PSCK of EYECAM chip U215 provides signal PSClk, which is the power supply clock. The

power supply clock is used to control the DC to DC converter depicted in Figure 7.

Output pins CTO0-CTO2 of EYECAM chip U215 are general purpose output pins which are not used in this camera. Other cameras could for example use output pins CTO0-CTO2 to control LEDs, relays, or any other function that requires a digital control line. Output pins CTO0-CTO2 are controlled through the built in I2C interface of EYECAM chip U215.

Output pin CDCL of EYECAM chip U215 provides clamping signal CDS-CLMP, which controls the clamping of the input signal to CDS chip U110. The timing of clamping signal CDS-CLMP is controlled by output pin CLHO in conjunction with capacitor C215 and resistor R234. Specifically, output pin CLHO controls the delay between the falling edge of clamp signal CDS-CLMP and the edges of signals H1 and H2. Increasing the RC time constant of capacitor C215 and resistor R234 will increase the delay between the edges.

Output pin CDSA of EYECAM chip U215 provides sample and hold signal CDS-S/H, which controls the timing of CDS chip U110. The timing of sample and hold signal CDS-S/H is controlled by output pin SAHO in conjunction with capacitor C216 and resistor R235. Specifically, output pin SAHO controls the delay between the falling edge of sample and hold signal CDS-S/H and the edges of reset gate signal RG. Increasing

the RC time constant of capacitor C216 and resistor R235 will increase the delay between the edges.

Output pin RSGT of EYECAM chip U215 provides sample and reset gate signal RG, which clears the charge amplifier in CCD U101. The timing of reset gate signal RG is controlled by output pin RGHO in conjunction with capacitor C217 and resistor R236. Specifically, output pin RGHO controls the delay between the falling edge of reset get signal RG and the edge of clamp signal CDS-CLMP. Increasing the RC time constant of capacitor C217 and resistor R236 will increase the delay between the edges.

Input pin HNL of EYECAM chip U215 determines whether a high resolution CCD or a low resolution CCD is used in the camera. Specifically, if a logic high is coupled to input pin HNL, EYECAM chip U215 assumes a high resolution CCD is used; otherwise, EYECAM chip U215 assumes a low resolution CCD is used. Resistors R237 and R238 determine the state of input pin HNL. Only one of the resistors is actually present on the board. In this embodiment R237 is not stuffed (NS) so that the coupling of resistor R238 to ground pulls input pin HNL low.

Similarly, input pin PNN of EYECAM chip U215 determines whether the CCD uses NTSC or PAL video timing. Specifically, if a logic high is coupled to

input pin PNN, EYECAM chip U215 assumes a PAL CCD is used; otherwise, EYECAM chip U215 assumes a NTSC CCD is used. Resistors R239 and R240 determine the state of input pin PNN. Only one of the resistors is actually present on the board. In this embodiment R239 is not stuffed (NS) so that the coupling of resistor R240 to ground pulls input pin PNN low.

Connectors P1A and P201 are coupled the optical capture board of Figure 5. Connector P18 is coupled to the power supply board of Figure 7. The power supply board of Figure 7 also contains EEPROM U301 and DAC chip U302.

EEPROM U301 is an I2C EEPROM manufactured by Signetics with part number PCF8582. EEPROM U301 corresponds to memory device 210 (Figure 2(a)). Pins SCL and SDA of EEPROM U301 are the filtered I2C clock and data line, respectively. Address pins A2, A1, and A0 are offset address pins to change the I2C address of EEPROM U301. In this implementation, the address pins are connected to ground. Ground pin GND is also connected to ground. Power pin VCC is connected to power signal +5V. Input Pin RC is used to control the timing of EEPROM U301. The values of resistor R301 and capacitor C301 determine write timing as detailed in the data sheet for PCF8582 available from Signetics.

DAC chip U302, corresponding to digital-to-analog converter 212 (Figure 2(a)), is an I2C

digital-to-analog converter available from Signetics with part number TDA8444T. Pins SCL and SDA of DAC chip U302 are the filtered I2C clock and data line respectively. DAC chip U302 is controlled by computer system 250 (Figure 2(a)) through the I2C interface. DAC chip U302 provides 6 bits of resolution. Address pins A0-A2 are offset address pins to change the I2C address of EEPROM U301. In this camera, the address pins are connected to ground. Ground pin GND is also connected to ground. Power pin VCC is connected to a +12 volt line. The +12 volt line is generated from power signal +15VUF through resistor R302 with 12 volt zener diode D301. Capacitors C302 and C303 filters the +12 volt line. Input pin VMAX, which determines the maximum value of the output signals is set to 10 volts using the +12 volt line and voltage divider resistors R303 and R304. Capacitor C304 provides filtering on the +10 volt line.

Although DAC chip U302 has eight DAC output pins DAC0-DAC7. Only four of the DAC output pins are used in this implementation. Output pin DAC0 provides signal BIAS. Resistors R320, R310, and R330 constrain the value of signal BIAS to between .54 volts and 2.49 volts. Output pin DAC1 provides signal RG-C, the reset gate average level adjustment, to CCD U101 as described above with respect to Figure 5. The range of signal RG-C is between 0.3 volts and 6.0 volts; therefore, no

external scaling resistors are required. Output pin DAC2 provides signal A/D-GAIN to ADC chip U205. Resistors R312, R322, and R332 constrain the value of signal A/D-GAIN to between 1.75 volts and 4.11 volts. Output DAC7 provides signal CDS-GAIN to CDS chip U110. Resistors R317, R327, and R337 constrain the value of signal CDS-GAIN to between 1.13 volts and 3.28 volts.

Signal BIAS from output pin DAC0 of DAC chip U302 is converted to substrate bias signal SUB, which is coupled to CCD U101. Signal BIAS is connected to the base of transistor Q3, a conventional amplifier, which in this implementation has part number 2N3904. Power signal +15VA is boosted by the dual diode package D340, capacitor C342, and capacitor C343, a positive level clamper driven by signal OV2. Signal OV2 from VDRIVE chip U121 deviates between -9 volts and 0 volts. Thus the voltage on the collector of transistor Q3 is the sum of power signal +15VA with 9 volts from capacitor C342 minus the voltage drop across the diodes. This produces a voltage of approximately 22-23 volts across capacitor C343. Resistor R340 is a collector load resistor, while resistor R341 is an emitter gain resistor. Capacitor C344 provides filtering to the base of transistor Q340. Signal SUB from the emitter of Q340 is inversely proportional to signal BIAS. However, signal SUB will range between 8 volts and 18 volts. Resistors R342 is an emitter resistor.

Diode 341 allows the substrate pulses on signal SUB to appear on input pin OFD of CCD U101 (Figure 5). Resistor R343 filters signal SUB.

Power chip U350, which is a Linear Technology LT1172CS8-5 DC to DC power converter, provides the various voltage levels required by the components in the Camera. Input pin VIN, of Power chip U350, receives power signal +5V through inductor L350 and diode D350. If the voltage in input pin VIN drops below 3.3 volts, power chip U350 shuts down. Capacitor C350 provides filtering on power signal +5V. Signal PSClk from EYECAM chip U215 (Figure 6) is current limited through resister R350 and drives transistor Q350 with biasing resistor R351. Input pin VC is connected to the collector of Q350 and the pole-zero compensation network formed by resister R352 and capacitor C351. Pins E1 and E2 as well as ground pin GND must be connected to ground.

Output pin VSW of power chip U350 pulls pin 3 of transformer T350 to ground to charge the magnetic field in transformer T350. When output pin VSW turns off, the magnetic field in transformer T350 collapses. The energy stored in transformer T350 moves to capacitor C357 through diode D351, thus developing power signal +15VUF. Power signal +15VUF, is connected to feedback input pin FB through voltage divider resistors R354 and R353. The values of resistors R354

and R353 are chosen so that a voltage of approximately +15 volts is scaled to a voltage of approximately 1.24 volts on feedback input pin FB. If the signal on feedback input pin FB rises above approximately 1.24 volts power chip U350 stores less energy in transformer T350. Therefore power chip U350 regulates power signal +15VUF to approximately +15 volts. Inductor L360 filters power signal +15VUF to produce power signal +15VA.

Diode D353 is a negative level clamper and voltage doubler, that develops a voltage of -15 volts at capacitor C356. LED D254 provides a 1.4 volt drop and resister R355 limits the current through nine volt zener diode D101 (Figure 5). Nine volt Zener diode D101 (Figure 5) regulates power signal -9VA to -9 volts.

By using the 10 volt middle tap of transformer T350, half wave rectifier D352 creates a 8.5-9 volt power signal across capacitor C353. Resister R356 and inductor L340 filters the 8.5-9 volt power signal to produce power signal +8VUR, that is used by voltage regulator U201 (Figure 6) to generate power signal +5VA.

Connecter P301 of the power supply board is coupled to connector P201 of the control board.

As explained above, computer system 250 (Figure 2(a)) controls the camera depicted in

Figures 5-7 through an I2C serial interface on interface J202 (Figure 6). Computer system 250 is able to control the analog signal gain, scan rate, exposure time, frame rate, and conversion rate of the camera depicted in Figures 5-7. Specifically, computer system 250 controls the analog signal gain by controlling signal CDS-GAIN through DAC chip U302. By controlling EYECAM chip U215, computer system 250 can control the scan rate and exposure time of CCD U101 as explained above. Furthermore, control of EYECAM chip U215 allows computer system 250 to dictate the frame rate of the outgoing video signal, as well as to control signal Adclk and thereby control the conversion rate of ADC chip U205.

Thus by using a digital video camera according to the principles of this invention, a computer system is able to dictate the frame rate, scan rate, resolution, exposure time and analog signal gain of the digital video camera. Control of the frame rate and resolution of the digital video camera allows the computer system to tailor the video sequence to the constraints of the computer system rather than the dictates of analog video standards. Furthermore, by independently controlling exposure time, scan rate, and analog signal gain the computer system can use the optical sensor of the digital video camera as an analog frame buffer to obtain temporal smoothing within each frame of the

video sequence. The resulting video sequence is smoother than can be obtained from conventional video cameras. Furthermore, the digital video output of the digital video camera eliminates an analog-to-digital conversion step, which is necessary for a computer system to use conventional video cameras. Elimination of the extra conversion step results in a cleaner video sequence.

The various embodiments of the structure and method of this invention that are described above are illustrative only of the principles of this invention and are not intended to limit the scope of the invention to the particular embodiments described. In view of this disclosure, those skilled-in-the-art can define other optical sensors, interfaces, video processors, other components and use these alternative features to create a method or system of digital video capturing according to the principles of this invention.

CLAIMS

We claim:

1. A digital video camera comprising:

an optical sensor having a first horizontal resolution and a first vertical resolution, adapted to capture a first image at a controllable exposure time, wherein said first image has a second horizontal resolution and a second vertical resolution;

an amplifying element coupled to said optical sensor for transforming said first image into a second image;

an analog-to-digital converter coupled to said amplifying element for converting said second image into a first digital image;

a video processor coupled to said analog-to-digital converter for transforming said first digital image into a digital output image; and

a digital output interface for receiving said digital output image from said video processor and for outputing said digital output image from said digital video camera.

2. The digital video camera of claim 1, wherein said second horizontal resolution is less than said first horizontal resolution.

3. The digital video camera of claim 1, wherein said second vertical resolution is less than said first vertical resolution.

4. The digital video camera of claim 1, wherein said digital output image has a third horizontal resolution and a third vertical resolution.

5. The digital video camera of claim 4, wherein said third horizontal resolution is less than said second horizontal resolution.

6. The digital video camera of claim 4, wherein said third vertical resolution is less than said second vertical resolution.

7. The digital video camera of claim 1, wherein said optical sensor comprises a two dimensional array of photodiodes.

8. The digital video camera of claim 1, wherein said optical sensor comprises a two dimensional array of CCDs.

9. The digital video camera of claim 1, wherein said analog-to-digital converter operates at a conversion rate independent of said exposure time.

10. The digital video camera of claim 1, wherein said amplifying element has an alterable signal gain.

11. The digital video camera of claim 1, wherein said optical sensor is adapted to repeatedly capture a plurality of sequential first images at an alterable scan rate.

12. The digital video camera of claim 11, wherein said optical sensor has a controllable exposure time independent of said alterable scan rate; thereby allowing said optical sensor to perform temporal smoothing of each of said first images independent of said alterable scan rate.

13. The digital video camera of claim 11 wherein

said amplifying element is adapted to transform each of said first images into said second image; and

said digital output interface is adapted to output said digital output image at an alterable output frame rate.

14. The digital video camera of claim 11 further comprising a control interface, wherein one or more signals provided to said digital video camera through said control interface set said alterable scan rate.

15. The digital video camera of claim 1, further comprising a control interface, wherein one or more signals provided to said digital video camera through said control interface set said second horizontal dimension and said second vertical dimension.

16. The digital video camera of claim 4, further comprising a control interface, wherein one or more signals provided to said digital video camera through said control interface set said third horizontal dimension and said third vertical dimension.

17. The digital video camera of claim 1, further comprising a control interface, wherein one or more signals provided to said digital video camera through said control interface set said controllable exposure time.

18. The digital video camera of claim 13, further comprising a control interface, wherein one or more signals provided to said digital video camera through said control interface set said alterable output frame rate.

19. The digital camera of claim 13, wherein said alterable scan rate is 30 images per second.

20. The digital camera of claim 11, wherein said alterable scan rate is 20 images per second.

21. The digital camera of claim 12, wherein said alterable scan rate is 15 images per second.

22. The digital video camera of claim 10, further comprising a control interface, wherein one or more signals provided to said digital video camera through said control interface set said alterable signal gain.

23. The digital video camera of claim 1, further comprising a memory containing a plurality of calibration datum for said digital video camera.

24. The digital video camera of claim 23, further comprising an auxiliary interface for reading said memory.

25. The digital video camera of claim 24, wherein said auxiliary interface is an I2C serial bus.

26. The digital video camera of claim 24, wherein said auxiliary interface and said digital output interface form a single interface.

27. The digital video camera of claim 1, wherein

said digital output device is connected to a processor based system.

28. The digital video camera of claim 27, wherein said processor based system is a computer.

29. The digital video camera of claim 27, wherein said processor based system is a video phone.

30. The digital video camera of claim 14, wherein said digital output interface and said controller interface form a single interface.

31. A method of creating a digital video sequence comprising

controlling an exposure time on an optical sensor;

capturing a plurality of analog images with said optical sensor;

amplifying each of said analog images into an amplified image thus forming a plurality of amplified images;

converting each of said amplified images into a digital image thus forming a plurality of digital images; and

processing each of said digital images into a processed digital image thus forming a plurality

of processed images; and

outputing each of said processed digital images on a digital output interface.

32. The method of Claim 31, wherein said converting each of said analog images into a digital image further comprises:

assigning an alterable scan rate for said converting each of said analog images into a digital image.

33. The method of claim 32, wherein said processing each of said digital images into a processed digital image further comprises:

resizing each of said digital images.

34. Structure for creating a video sequence comprising:

means for controlling an exposure time on an optical sensor;

means for capturing a plurality of analog images with said optical sensor;

means for amplifying each of said analog images into an amplified image thus forming a plurality of amplified images;

means for converting each of said amplified images into a digital image thus forming a

plurality of digital images; and

means for processing each of said digital images into a processed digital image thus forming a plurality of processed images; and

means for outputing each of said processed digital images on a digital output interface.

35. The structure of Claim 34, wherein said means for converting each of said analog images into a digital image further comprises:

means for assigning an alterable scan rate for said converting each of said analog images into a digital image.

36. The structure of claim 35, wherein said means for processing each of said digital images into a processed digital image further comprises:

means for resizing each of said digital images.

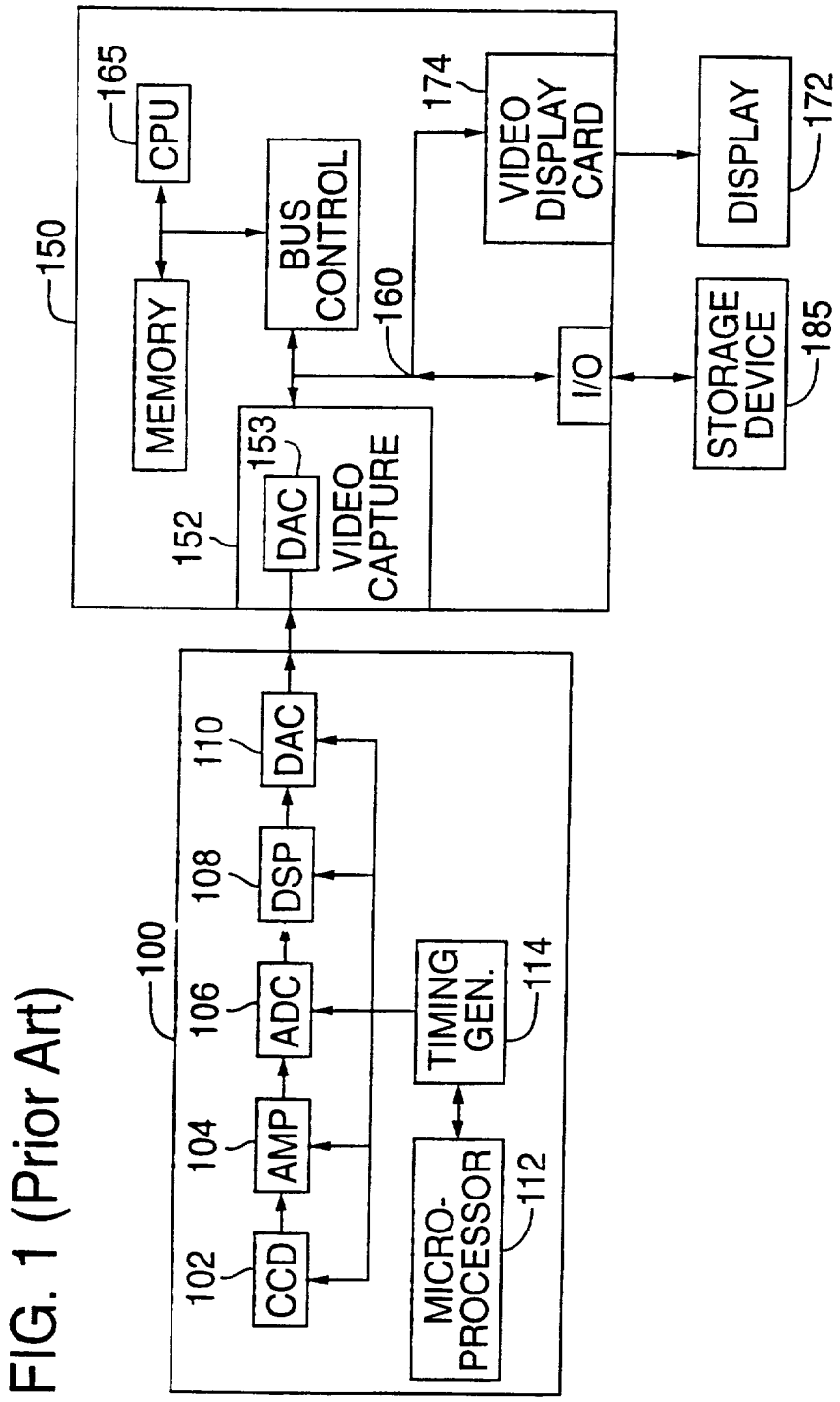


FIG. 1 (Prior Art)

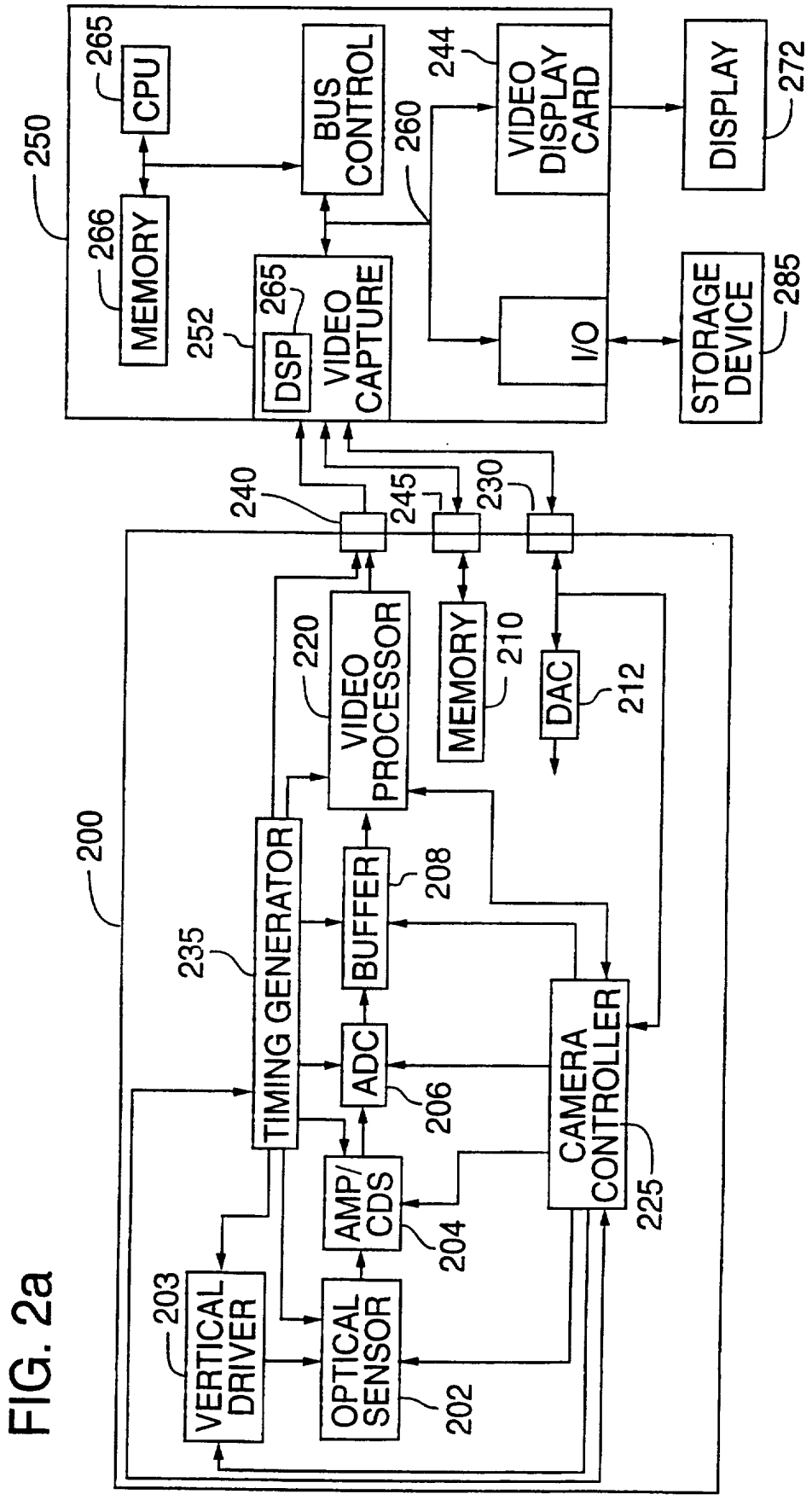
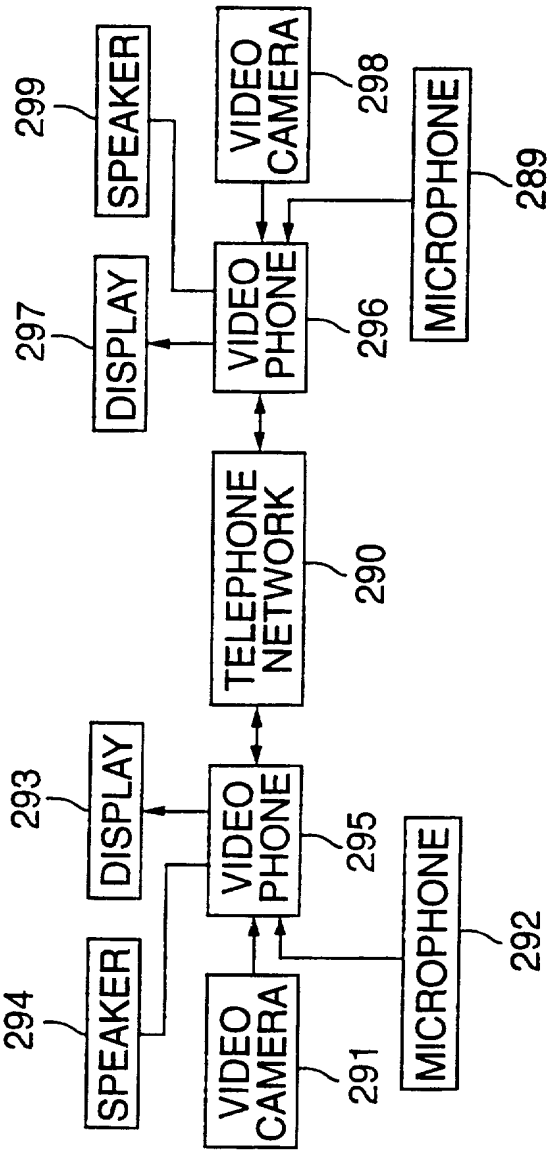

250
265
CPU
266
MEMORY
BUS CONTROL
260
244
VIDEO DISPLAY CARD
DISPLAY
272
252
DSP
265
VIDEO CAPTURE
I/O
STORAGE DEVICE
285
240
245
230
200
VIDEO PROCESSOR
220
MEMORY
210
DAC
212
TIMING GENERATOR
235
BUFFER
208
ADC
206
AMP/ CDS
204
CAMERA CONTROLLER
225
VERTICAL DRIVER
203
OPTICAL SENSOR
202

FIG. 2a

FIG. 2b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299
VIDEO CAMERA
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DISPLAY
297
VIDEO PHONE
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MICROPHONE
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MICROPHONE
292

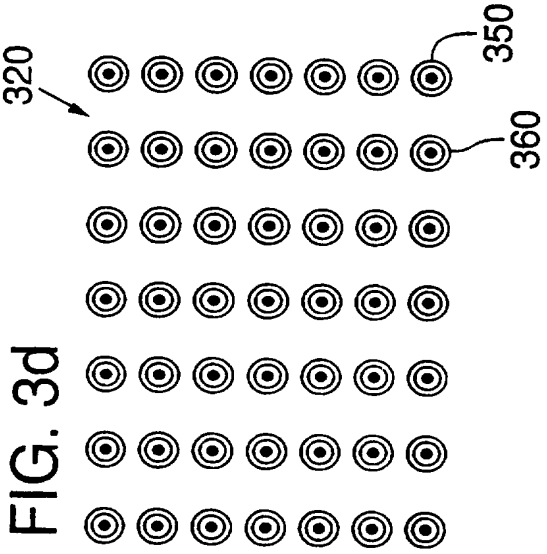


FIG. 3d

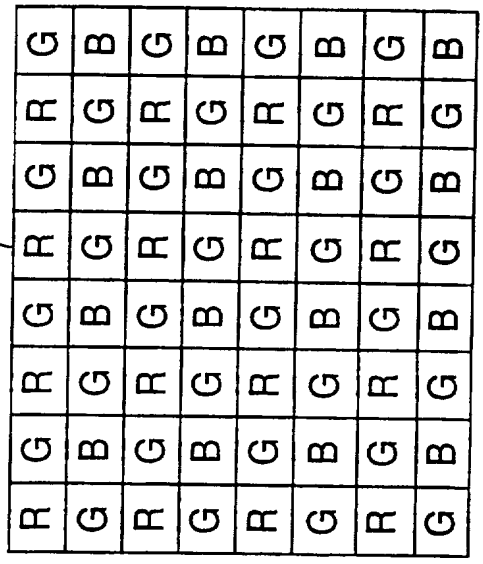


FIG. 3c

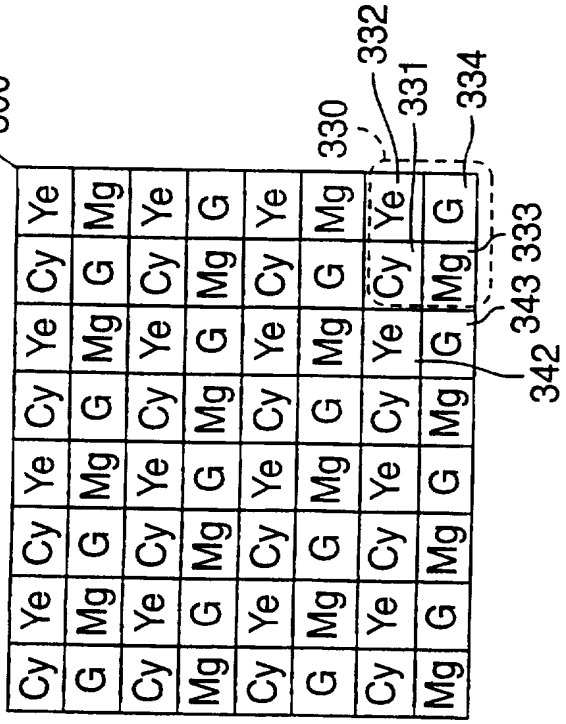


FIG. 3a

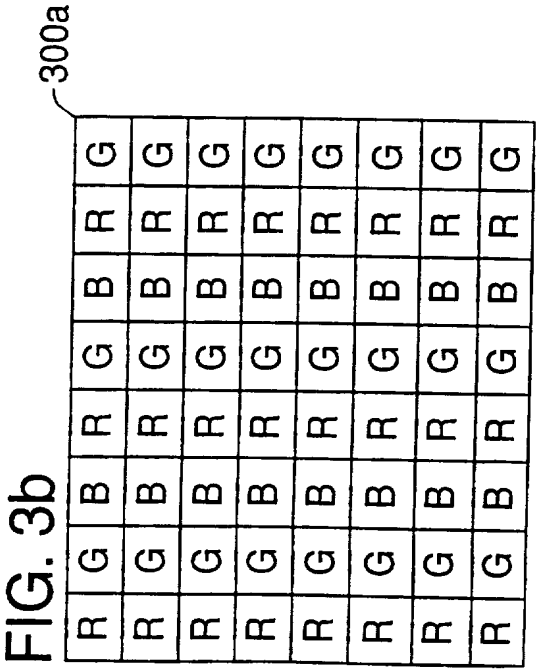


FIG. 3b

FIG. 4a

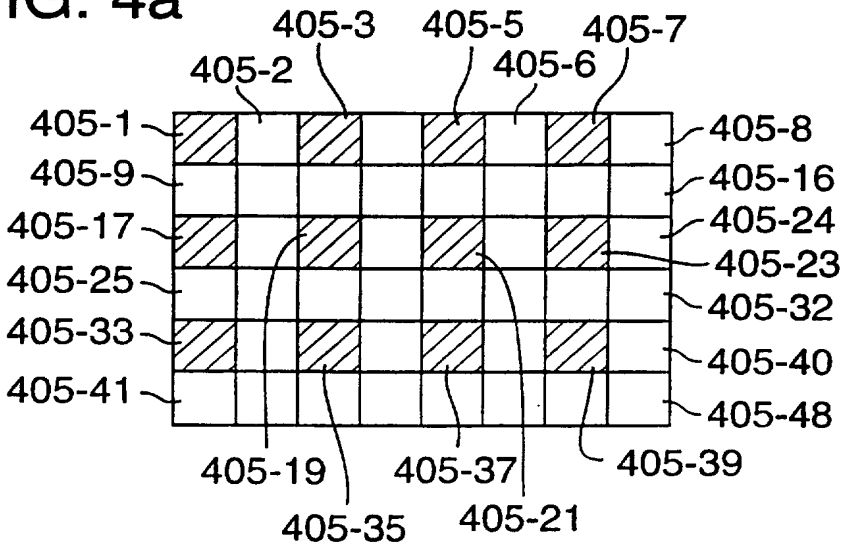


FIG. 4b

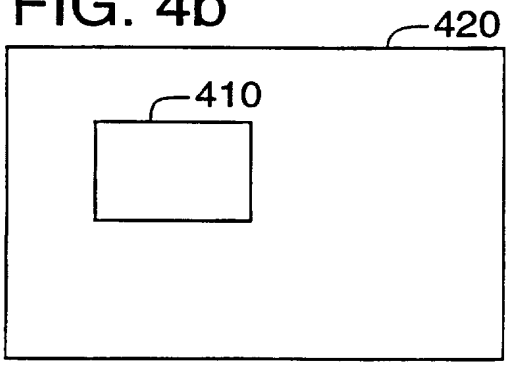


FIG. 4d

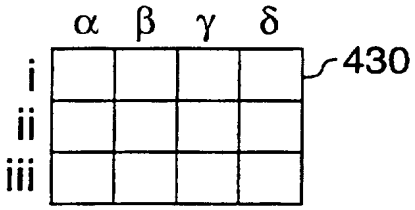
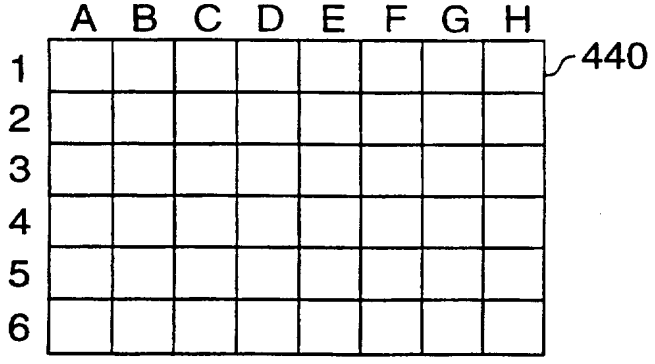


FIG. 4c



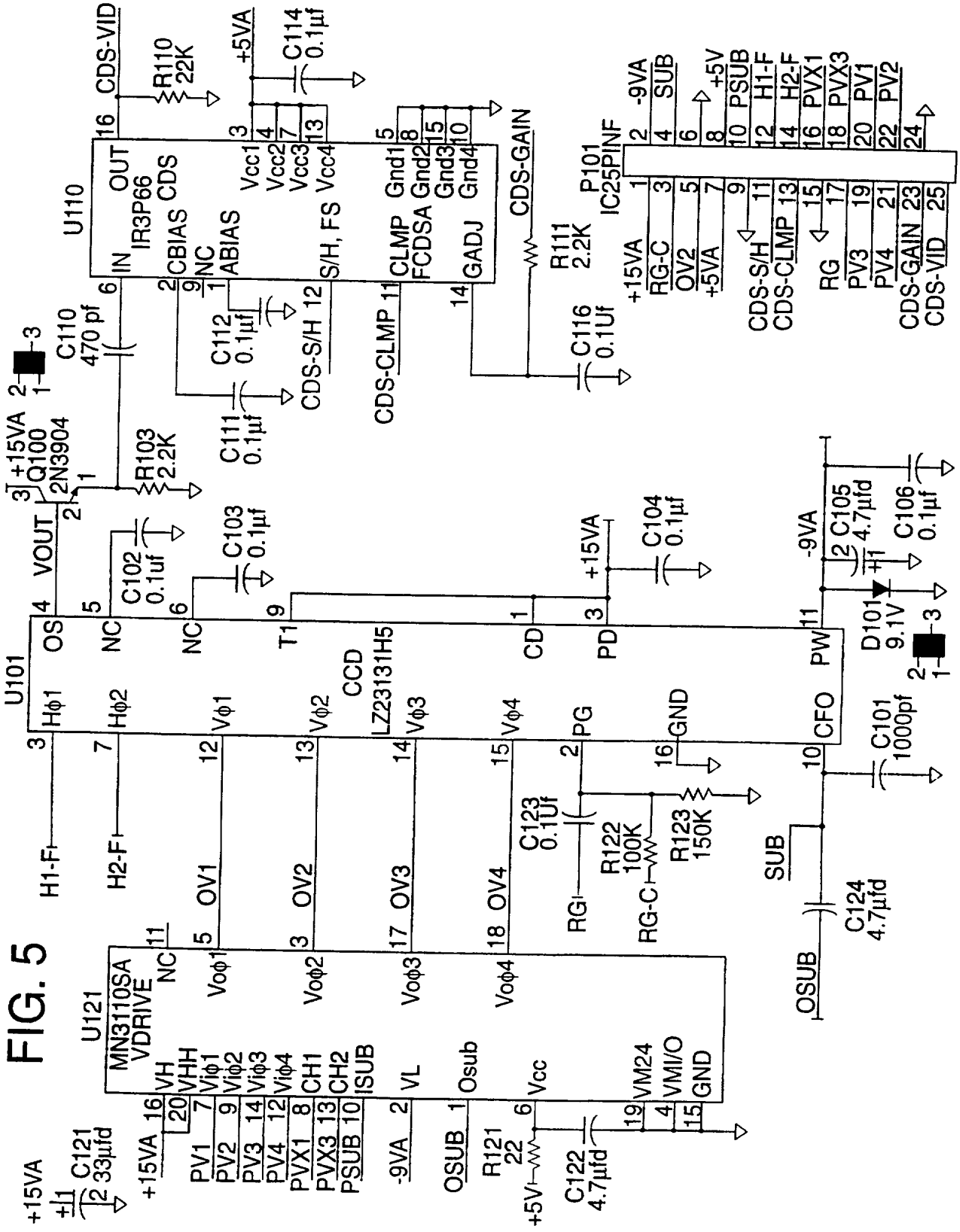

U110
IR3P66
IN
OUT
CDS
CBIAS
NC
ABIAS
Vcc1
Vcc2
Vcc3
Vcc4
S/H, FS
CLMP
FCDSA
Gnd1
Gnd2
Gnd3
Gnd4
GADJ
CDS-VID
R110 22K
+5VA
C114 0.1µf
C110 470 pf
C112 0.1µf
C111 0.1µf
CDS-S/H 12
CDS-CLMP 11
CDS-GAIN
R111 2.2K
C116 0.1Uf
P101 IC25PINF
-9VA
SUB
+5V
PSUB
H1-F
H2-F
PVX1
PVX3
PV1
PV2
+15VA
RG-C
OV2
+5VA
CDS-S/H
CDS-CLMP
RG
PV3
PV4
CDS-GAIN
CDS-VID
Q100 2N3904
R103 2.2K
C103 0.1µf
C102 0.1uf
C104 0.1µf
C105 4.7µfd
C106 0.1µf
D101 9.1V
U101
CCD
LZ23131H5
VOUT
OS
NC
T1
CD
PD
PW
Hφ1
Hφ2
Vφ1
Vφ2
Vφ3
Vφ4
PG
GND
CFO
OV1
OV3
OV4
C101 1000pf
C123 0.1Uf
R122 100K
R123 150K
SUB
C124 4.7µfd
OSUB
U121
MN3110SA
VDRIVE
VH
VHH
Viφ1
Viφ2
Viφ3
Viφ4
CH1
CH2
ISUB
VL
Osub
Vcc
VM24
VMI/O
GND
Voφ1
Voφ2
Voφ3
Voφ4
PV1
PV2
PV3
PV4
PVX1
PVX3
PSUB
-9VA
OSUB
R121 22
C122 4.7µfd
+5V
+15VA
C121 33µfd

FIG. 5

FIG. 6A

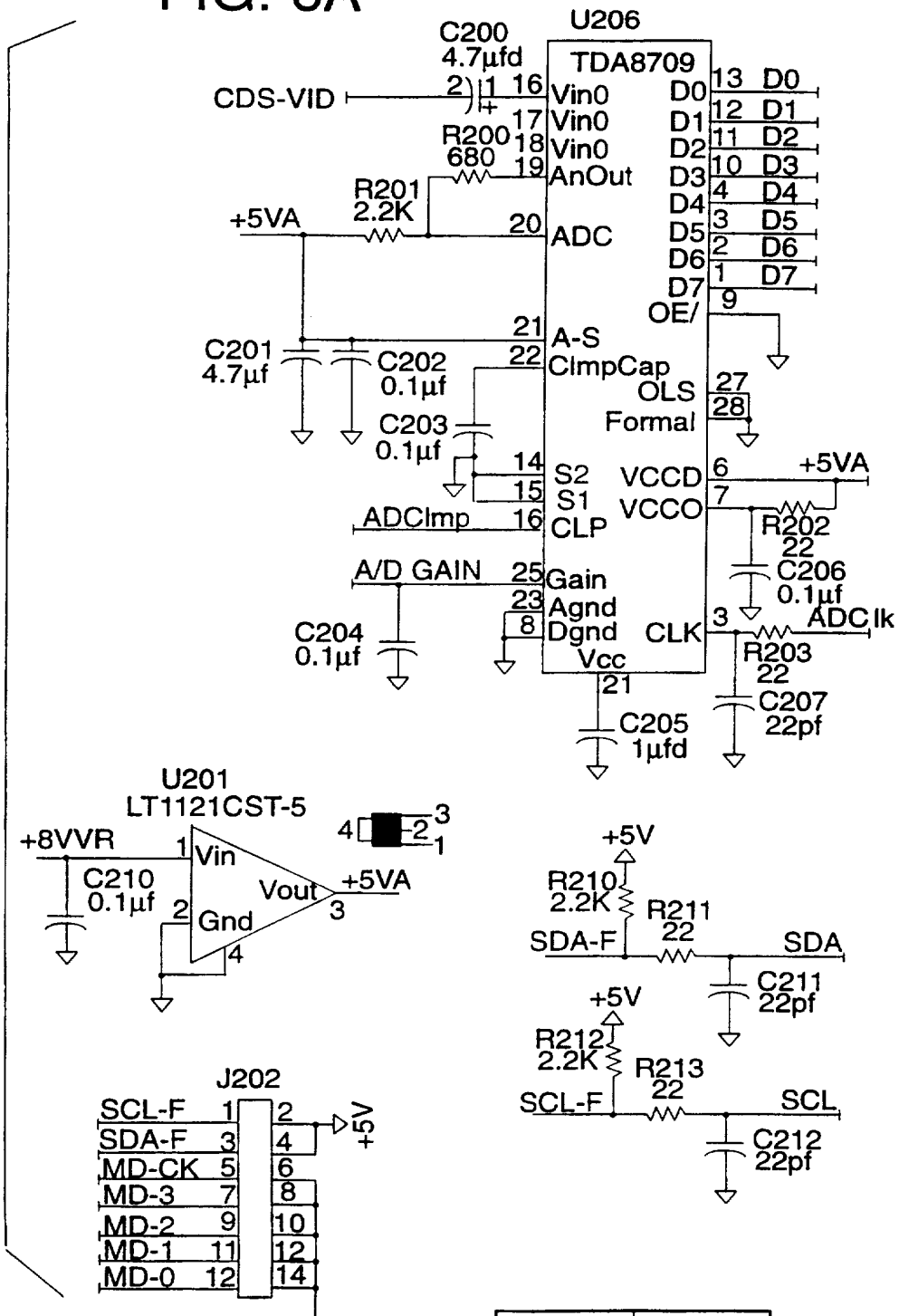


FIG. 6A	FIG. 6B

Key to Figure 6

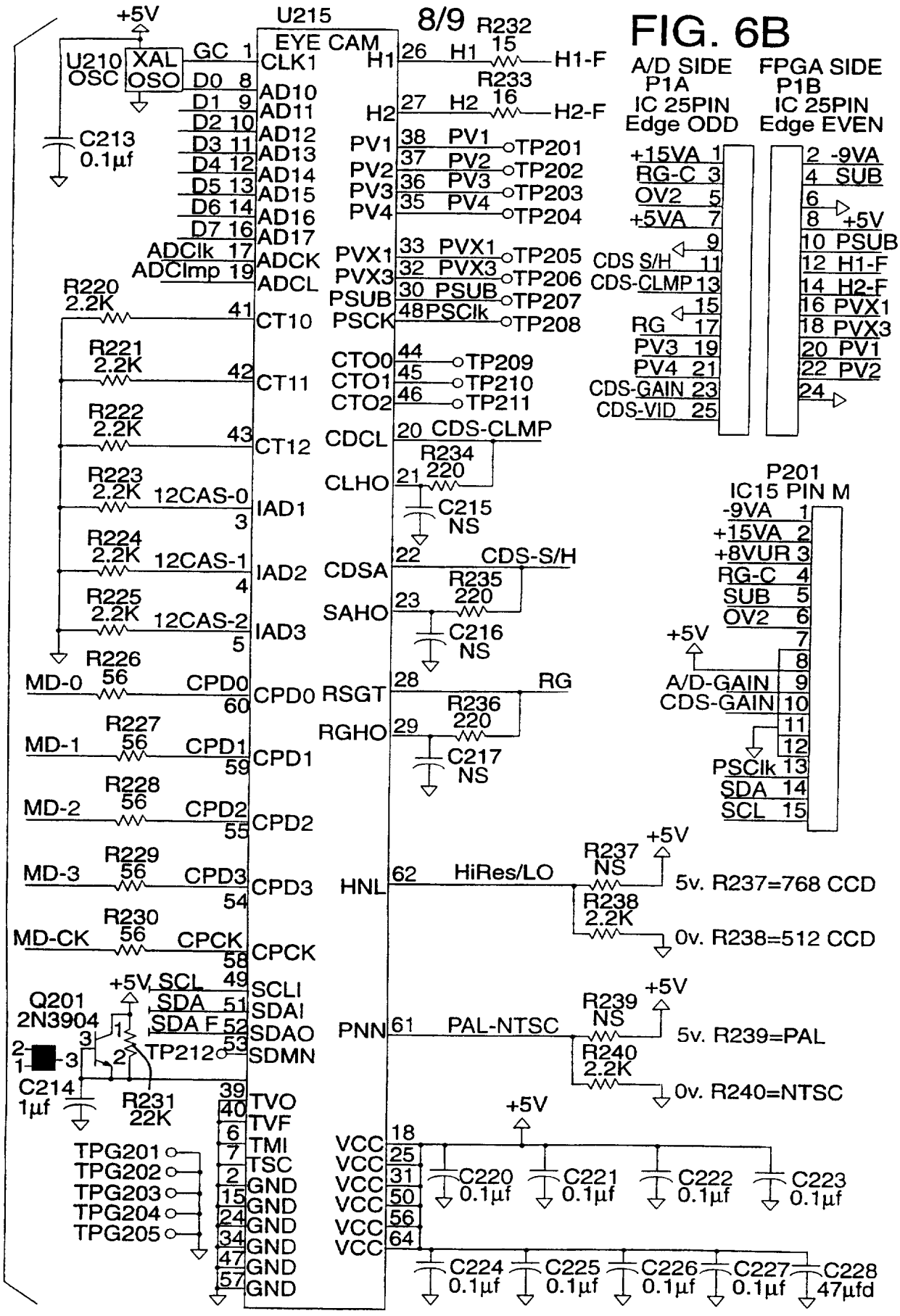
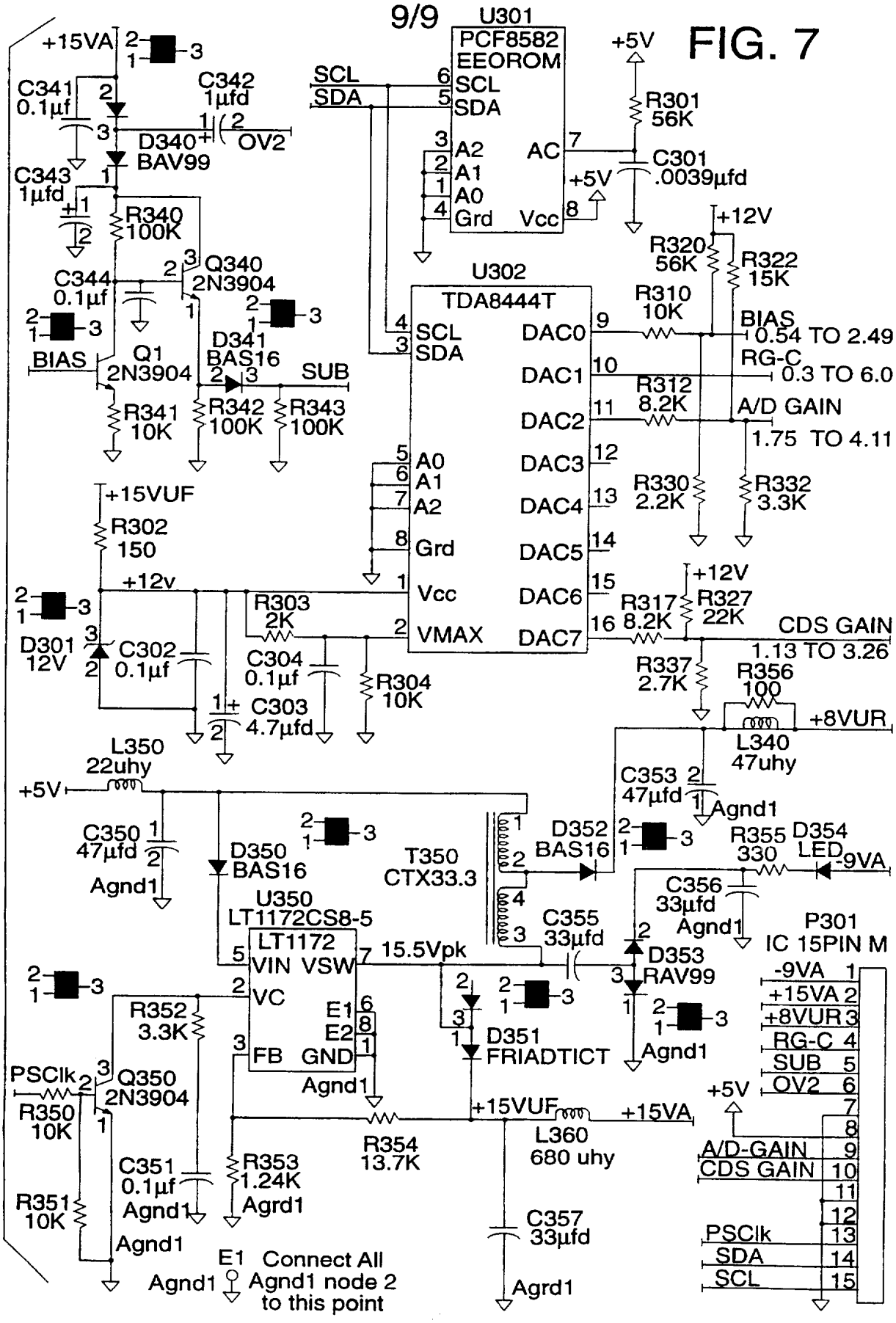


FIG. 6B
8/9
U215
EYE CAM
A/D SIDE P1A IC 25PIN Edge ODD
FPGA SIDE P1B IC 25PIN Edge EVEN
P201 IC15 PIN M
+5V
U210 OSC
XAL
OSO
C213 0.1µf
GC 1 CLK1
D0 8 AD10
D1 9 AD11
D2 10 AD12
D3 11 AD13
D4 12 AD14
D5 13 AD15
D6 14 AD16
D7 16 AD17
ADClk 17 ADCK
ADCImp 19 ADCL
R220 2.2K
R221 2.2K
R222 2.2K
R223 2.2K 12CAS-0
R224 2.2K 12CAS-1
R225 2.2K 12CAS-2
R226
MD-0 56 CPD0
R227
MD-1 56 CPD1
R228
MD-2 56 CPD2
R229
MD-3 56 CPD3
R230
MD-CK 56 CPCK
Q201 2N3904
TP212
C214 1µf
R231 22K
TPG201
TPG202
TPG203
TPG204
TPG205
SCL 49 SCLI
SDA 51 SDAI
SDA F 52 SDAO
53 SDMN
39 TVO
40 TVF
6 TMI
7 TSC
2 GND
15 GND
24 GND
34 GND
47 GND
57 GND
H1 26 H1 15 H1-F
R233
H2 27 H2 16 H2-F
PV1 38 PV1 TP201
PV2 37 PV2 TP202
PV3 36 PV3 TP203
PV4 35 PV4 TP204
PVX1 33 PVX1 TP205
PVX3 32 PVX3 TP206
PSUB 30 PSUB TP207
PSCK 48 PSClk TP208
CTO0 44 TP209
CTO1 45 TP210
CTO2 46 TP211
CDCL 20 CDS-CLMP
R234 220
CLHO 21
C215 NS
22 CDS-S/H
CDSA
R235 220
SAHO 23
C216 NS
28 RG
RSGT
R236 220
RGHO 29
C217 NS
HNL 62 HiRes/LO
R237 NS
5v. R237=768 CCD
R238 2.2K
0v. R238=512 CCD
PNN 61 PAL-NTSC
R239 NS
5v. R239=PAL
R240 2.2K
0v. R240=NTSC
VCC 18
VCC 25
VCC 31
VCC 50
VCC 56
VCC 64
C220 0.1µf
C221 0.1µf
C222 0.1µf
C223 0.1µf
C224 0.1µf
C225 0.1µf
C226 0.1µf
C227 0.1µf
C228 47µfd
+15VA 1
RG-C 3
OV2 5
+5VA 7
9
CDS S/H 11
CDS-CLMP 13
15
RG 17
PV3 19
PV4 21
CDS-GAIN 23
CDS-VID 25
2 -9VA
4 SUB
6
8 +5V
10 PSUB
12 H1-F
14 H2-F
16 PVX1
18 PVX3
20 PV1
22 PV2
24
-9VA 1
+15VA 2
+8VUR 3
RG-C 4
SUB 5
OV2 6
+5V 7
8
A/D-GAIN 9
CDS-GAIN 10
11
12
PSClk 13
SDA 14
SCL 15

FIG. 7


U301
PCF8582
EEOROM
SCL
SDA
A2
A1
A0
Grd
Vcc
AC
+5V
+15VA
C341
0.1µf
C342
1µfd
OV2
D340
BAV99
C343
1µfd
R340
100K
Q340
2N3904
C344
0.1µf
BIAS
Q1
2N3904
D341
BAS16
SUB
R341
10K
R342
100K
R343
100K
R301
56K
C301
.0039µfd
+12V
R320
56K
R322
15K
U302
TDA8444T
R310
10K
BIAS
0.54 TO 2.49
RG-C
0.3 TO 6.0
R312
8.2K
A/D GAIN
1.75 TO 4.11
DAC0
DAC1
DAC2
DAC3
DAC4
DAC5
DAC6
DAC7
VMAX
R330
2.2K
R332
3.3K
+15VUF
R302
150
+12v
D301
12V
C302
0.1µf
R303
2K
C304
0.1µf
R304
10K
C303
4.7µfd
R317
8.2K
R327
22K
CDS GAIN
1.13 TO 3.26
R337
2.7K
R356
100
+8VUR
L340
47uhy
L350
22uhy
C353
47µfd
Agnd1
C350
47µfd
D350
BAS16
T350
CTX33.3
D352
BAS16
R355
330
D354
LED
-9VA
C356
33µfd
U350
LT1172CS8-5
LT1172
VIN
VSW
VC
E1
E2
FB
GND
15.5Vpk
C355
33µfd
D353
RAV99
D351
FRIADTICT
P301
IC 15PIN M
-9VA 1
+15VA 2
+8VUR 3
RG-C 4
SUB 5
OV2 6
A/D-GAIN 9
CDS GAIN 10
PSClk 13
SDA 14
SCL 15
R352
3.3K
PSClk
Q350
2N3904
R350
10K
R351
10K
C351
0.1µf
R353
1.24K
Agrd1
R354
13.7K
L360
680 uhy
C357
33µfd
E1 Connect All
Agnd1 node 2
to this point

INTERNATIONAL SEARCH REPORT

Intern. nal Application No
PCT/US 97/05838

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04N5/232

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04N

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 659 017 A (EASTMAN KODAK CO) 21 June 1995 see column 6, line 1 - line 12 see column 4, line 52 - column 5, line 20	1-10,31, 34
Y	---	11,12, 32,35
Y	EP 0 265 302 A (THOMSON CSF) 27 April 1988 see column 2, line 48 - column 3, line 8	11,12, 32,35
Y	---	11,12, 32,35
A	WO 91 08644 A (EASTMAN KODAK CO) 13 June 1991 see page 9, line 18 - line 37	1,4

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[X] Further documents are listed in the continuation of box C.

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2

Date of the actual completion of the international search	Date of mailing of the international search report
4 July 1997	17.07.97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax (+ 31-70) 340-3016	Bequet, T

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INTERNATIONAL SEARCH REPORT

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A	IEEE TRANSACTIONS ON CONSUMER ELECTRONICS, vol. 39, no. 3, 1 August 1993, pages 467-472, XP000396320 IMAIDE T ET AL: "A MULTIMEDIA COLOR CAMERA PROVIDING MULTI-FORMAT DIGITAL IMAGES" see the whole document ---	1,31,34
A	US 5 202 767 A (DOZIER DAVID R ET AL) 13 April 1993 see column 14, line 29 - line 49 ---	11,12, 32,35
A	US 5 479 206 A (UENO HITOSHI ET AL) 26 December 1995 see column 2, line 9 - line 16 see column 21, line 20 - line 67 -----	1,31,34

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Interna al Application No
PCT/US 97/05838

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0659017 A	21-06-95	JP 7240871 A	12-09-95
EP 0265302 A	27-04-88	FR 2604320 A	25-03-88
		DE 3779251 A	25-06-92
WO 9108644 A	13-06-91	US 5196938 A	23-03-93
		DE 69021198 D	31-08-95
		DE 69021198 T	11-04-96
		EP 0454842 A	06-11-91
		JP 4503145 T	04-06-92
US 4903132 A	20-02-90	JP 1084980 A	30-03-89
		US RE34654 E	05-07-94
US 5202767 A	13-04-93	NONE	
US 5479206 A	26-12-95	JP 5219428 A	27-08-93
		JP 5219429 A	27-08-93
		JP 5219430 A	27-08-93
		JP 5219422 A	27-08-93
		JP 5260398 A	08-10-93